Claims

That which is claimed:

1. A control system, comprising:

a digital control unit that is configured to generate a digital value responsive to a difference between an output analog value and a reference value;

a control signal generating unit that is configured to generate a control signal; and

an analog control unit that comprises a first circuit that is configured to generate a first analog value responsive to the digital value and a second circuit that is configured to generate a second analog value responsive to the control signal, the second circuit being configured to generate the second analog value at a resolution that is twice that of a resolution of the first circuit with respect to a least significant bit of the digital value, the analog control unit being configured to combine the first and second analog values to generate the output analog value.

2. The control system of Claim 1, further comprising:

a counting unit that comprises first and second counters that are configured to generate first and second counts, respectively, responsive to a clock signal, an evaluation signal, and the difference between the output analog value and the reference value;

wherein the digital control unit is configured to generate the digital value responsive to the first and second counts; and

wherein the control signal generating unit is configured to generate the control signal responsive to the evaluation signal.

3. The control system of Claim 2, wherein the first counter is configured to increase the first count when the reference value exceeds the output analog value and to maintain the first count otherwise; and

wherein the second counter is configured to increase the second count when the reference value exceeds the output analog value and to decrease the second count otherwise.

4. The control system of Claim 3, wherein the digital control unit is further configured to generate the digital value as an average of the first and second counts rounded down to the nearest decimal if the first and second counts are different and to generate the digital value as the value of the first and second counts minus one if the first and second counts are identical.

5. The control system of Claim 4, wherein the digital control unit comprises:

a comparing unit that is configured to determine whether the first and second counts are different or identical;

a first calculating unit that is configured to compute the digital value as an average of the first and second counts rounded down to the nearest decimal responsive to a determination by the comparing unit that the first and second counts are different;

a second calculating unit that is configured to compute the digital value by subtracting one from the value of the first and second counts responsive to a determination by the comparing unit that the first and second counts are identical; and

a storage unit that is configured to store the digital value computed by the first or second calculating units.

6. The control system of Claim 2, wherein the control signal is a first control signal, the system further comprising:

a comparing unit that is configured to generate a second control signal that is indicative of the difference between the output analog value and the reference value, the first and second counters being responsive to the second control signal.

7. The control system of Claim 1, wherein the first circuit of the analog control circuit comprises a plurality of output buffers comprising a plurality of control transistors, respectively, the plurality of control transistors being responsive to the digital value; and

wherein the second circuit of the analog control circuit comprises a sub output buffer that comprises a sub control transistor, the sub control transistor being responsive to the control signal and being one-half the size of the control transistor that is responsive to the least significant bit of the digital value.

8. The circuit of Claim 7, wherein a ratio of a size of the sub-control transistor that is responsive to an nth bit of the digital value to the size of the control transistor that is responsive to the least significant bit of the digital value is 2^{n-1}:1, wherein the least significant bit corresponds to the 1st bit of the digital value.

9. The control system of Claim 7, wherein the plurality of control transistors and the sub control transistor are connected in parallel between an output pad and a reference potential, the output analog value being generated at the output pad.

10. A circuit, comprising:

a first circuit that is configured to generate a first analog value responsive to a digital value; and

a second circuit that is configured to generate a second analog value responsive to a control signal, the second circuit being configured to generate the second analog value at a resolution that is twice that of a resolution of the first circuit with respect to a least significant bit of the digital value, the analog control unit being configured to combine the first and second analog values to generate an output analog value.

11. The circuit of Claim 10, wherein the first circuit comprises a plurality of output buffers comprising a plurality of control transistors, respectively, the plurality of control transistors being responsive to the digital value; and

wherein the second circuit comprises a sub output buffer that comprises a sub control transistor, the sub control transistor being responsive to the control signal and being one-half the size of the control transistor that is responsive to the least significant bit of the digital value.

12. The circuit of Claim 11, wherein a ratio of a size of the sub-control transistor that is responsive to an nth bit of the digital value to the size of the control transistor that is responsive to the least significant bit of the digital value is 2^{n-1}:1, wherein the least significant bit corresponds to the 1st bit of the digital value.

13. A method of operating a control system, comprising:

generating a digital value responsive to a difference between an output analog value and a reference value;

generating a control signal;

generating a first analog value responsive to the digital value;

generating a second analog value responsive to the control signal at a resolution that is twice that of a resolution associated with a least significant bit of the digital value; and

generating the output analog value by combining the first and second analog values.

14. The method of Claim 13, further comprising:

generating first and second counts responsive to a clock signal, an evaluation signal, and the difference between the output analog value and the reference value;

wherein generating the digital value comprises generating the digital value responsive to the first and second counts; and

wherein generating the control signal comprises generating the control signal responsive to the evaluation signal.

15. The method of Claim 14, wherein generating the first count comprises increasing the first count when the reference value exceeds the output analog value and maintaining the first count otherwise; and

wherein generating the second count comprises increasing the second count when the reference value exceeds the output analog value and decreasing the second count otherwise.

16. The method of Claim 15, wherein generating the digital value comprises:

generating the digital value as an average of the first and second counts rounded down to the nearest decimal if the first and second counts are different; and

generating the digital value as the value of the first and second counts minus one if the first and second counts are identical.

17. A control system for performing analog control, comprising:

a counting unit, which counts a number of clock signals that are input while an evaluation signal is activated in response to a first control signal and, upon deactivation of the evaluation signal, outputs the counted number of clock signals as a first count value of n bits and a second count value of n bits;

a digital control unit, which compares the first count value and the second count value, performs a predetermined operation based on the comparison result, and outputs the operation result as a third count value of n bits; and

an analog control unit, which controls an analog value in response to the third count value and receives a second control signal of 1 bit that can control a half of a minimum analog value that varies in response to a minimum change in the third count value.

18. The control system of Claim 17, wherein the second control signal is generated upon deactivation of the evaluation signal.

19. The control system of Claim 17, further comprising a comparing unit which compares the analog value with a reference value and generates the first control signal.

20. The control system of Claim 17, wherein the counting unit comprises:

a first counter, which operates in response to the evaluation signal, counts up when the first control signal is at a first level, and outputs the count value as the first count value upon deactivation of the evaluation signal; and

a second counter, which operates in response to the evaluation signal, counts up when the first control signal is at the first level, counts down when the first control signal is at a second level, and outputs the count value as the second count value upon deactivation of the evaluation signal.

21. The control system of Claim 20, wherein the first counter and the second counter operate when the evaluation signal is activated, do not operate when the evaluation signal is deactivated, and are reset in response to a reset signal.

22. The control system of Claim 17, wherein the digital control unit comprises:

a comparing operation unit, which generates a first signal when the first count value and the second count value are different and generates a second signal when the first count value and the second count value are identical;

a first calculating unit, which, in response to the first signal, sums the first count value and the second count value, obtains an average value of the sum of the first count value and the second count value, and generates a first calculation value by rounding down the average value;

a second calculating unit, which, in response to the second signal, generates a second calculation value by subtracting 1 from the first count value as a second calculation value; and

a storing unit, which stores the first calculation value or the second calculation value and generates the stored value as the third count value.

23. The control system of Claim 17, wherein the analog control unit comprises:

a first circuit, which controls the analog value in response to the third count value; and

a second circuit, which controls a half of a minimum analog value controlled by the first circuit in response to the second control signal.

24. The control system of Claim 17, wherein the analog control unit comprises:

first through n^{th} open drain output buffers, each of which includes a control transistor that is turned on or off in response to a respective bit of the third count value and a data transistor that receives data, connected in series, and controls the current through an output pad; and

a sub open drain output buffer, which includes a control transistor that is turned on or off in response to the second control signal and a data transistor that receives data, connected in series, and controls the current through the output pad.

25. The control system of Claim 24, wherein the size ratio of the first through n^{th} open drain output buffers is such that when the size of the control transistor of the first open drain output buffer is 1, the size of the control transistor of the n^{th} open drain output buffer is 2^{n-1}, and the size of the control transistor of the sub open drain output buffer is half of the control transistor of the first open drain output buffer.

26. A method of controlling an analog value, comprising:

comparing an analog value with a reference value and generating a first control signal at a first level or second level based on the comparison result;

counting the number of pulses of clock signals while an evaluation signal is activated in response to the first control signal and outputting the counted number of clock signals as a first count value of n bits and a second count value of n bits upon deactivation of the evaluation signal;

comparing the first count value and the second count value, performing a predetermined operation based on the comparison result, and outputting the operation result as a third count value of n bits; and

controlling the analog value in response to the third count value and receiving a second control signal of 1 bit that can control a half of a minimum analog value that varies in response to a minimum change in the third count value.

27. The method of Claim 26, wherein the second control value is generated upon deactivation of the evaluation signal.

28. The method of Claim 26, wherein counting the number of pulses further comprises:

counting up when the first control signal is at the first level and outputting the count value as the first count value upon deactivation of the evaluation signal; and

counting up when the first control signal is at the first level, counting down when the first control signal is at a second level, and outputting the count value as the second count value upon deactivation of the evaluation signal.

29. The method of Claim 26, wherein comparing the first count value and

the second count value further comprises:

comparing the first count value and the second count value to determine whether the first count value and the second count value are identical;

when the first count value and the second count value are not identical, summing up the first count value and the second count value, obtaining an average value of the summed result, and generating a first calculation value by rounding down the average value;

when the first count value and the second count value are identical, generating a second calculation value by deducting 1 from the first calculation value; and

storing the first calculation value or the second calculation value and generating the stored value as a third calculation value.

30. The method of Claim 26, wherein controlling the analog value further comprises:

controlling the analog value in response to the third count value; and

controlling a half of a minimum analog value that varies in response to the second control signal.

31. A method of controlling the current through an output pad connected to an output driver circuit that includes first through n^{th} open drain output buffers each of which includes a control transistor and a data transistor connected in series and a sub open drain output buffer which includes a control transistor and a data transistor connected in series, the method comprising:

determining whether the current through the output pad is closest to a reference current;

when the current through the output pad is closest to the reference current, determining a first digital signal of n bits that turns control transistors of the first through n^{th} open drain output buffers on or off;

controlling the current through the output pad by controlling the control transistors of the first through n^{th} open drain output buffers in response to the first digital signal of n bits; and

controlling the current through the output pad by controlling the control transistor of the sub open drain output buffer in response to a second digital signal.

32. The method of Claim 31, wherein determining the first digital signal comprises determining the first digital signal of n bits when the current through the output pad is less than and closest to the reference current.

33. The method of Claim 31, wherein the second digital signal increases the current through the output pad by turning on the control transistor of the sub open drain output buffer.

34. The method of Claim 31, wherein size of the control transistor of the sub open drain output buffer is half of the control transistor of the first open drain output buffer, and the size of the control transistor of the first open drain output buffer is least among the control transistors of the first through n^{th} open drain output buffers.